IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: **ROLANDI**

Serial No. **Not Yet Assigned**

Filing Date: **Herewith**

For: **INTEGRATED CIRCUIT FOR MEMORY CARD AND MEMORY CARD USING THE CIRCUIT**

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EXPRESS MAIL NO: EL747059413US

DATE OF DEPOSIT: June 14, 2001

NAME: Kyle Hopkinson

SIGNATURE:

PRELIMINARY AMENDMENT

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Drawings:

Submitted herewith is a request for proposed drawing modifications as indicated in red ink to label the blocks in FIGS. 1, 4-6, 8a-8b and 10. FIG. 10 is being further modified as indicated in red ink to correct a reference numeral.

In the Claims:

Please cancel Claims 1 to 32.

Please add new Claims 33 to 95.

33. An integrated circuit for storing data, and for application in a memory card that operates in cooperation with at least one of an external acquisition system and an external processing system, the integrated circuit comprising:

input/output means for receiving the data to be stored from at least one of the external acquisition system and the external processing system, for sending the stored data to the external processing system, and for receiving a command signal from at least one of the external acquisition system and the external processing system;

an electrically programmable non-volatile memory for storing the data in digital format, said electrically programmable non-volatile memory comprising a first terminal for receiving a programming signal for enabling storage of the data, and a second terminal for receiving a reading signal for enabling output of the stored data via said input/output means; and

memory control means connected to the first and second terminals of said electrically programmable non-volatile memory, and to said input/output means for generating the programming and reading signals based upon the command signal;

said electrically programmable non-volatile memory being erased by electromagnetic radiation for permitting a non-electrical erasure of the stored data.

34. An integrated circuit according to Claim 33, wherein the electromagnetic radiation comprises ultraviolet radiation.

35. An integrated circuit according to Claim 33,

wherein said integrated circuit comprises a single chip of semiconductor material.

36. An integrated circuit according to Claim 33, wherein said electrically programmable non-volatile memory comprises an erasable programmable read only memory (EPROM).

37. An integrated circuit according to Claim 33, said wherein said electrically programmable non-volatile memory comprises a multi-level architecture.

38. An integrated circuit according to Claim 33, wherein said electrically programmable non-volatile memory comprises a plurality of memory cells, each memory cell comprising a MOS transistor comprising a floating gate.

39. An integrated circuit according to Claim 33, wherein said electrically programmable non-volatile memory comprises a plurality of memory locations each corresponding to a respective address, and wherein said input/output means receives address signals corresponding to memory locations for storing the data or for reading the stored data.

40. An integrated circuit according to Claim 39, wherein said memory control means comprises:

an additional memory for storing a plurality of microinstructions for controlling said electrically programmable non-volatile memory; and

decoder means connected to said additional memory for converting the command signal to a selection signal for selecting at least one microinstruction.

41. An integrated circuit according to Claim 40, wherein said additional memory has a same physical structure as said electrically programmable non-volatile memory.

42. An integrated circuit according to Claim 40, wherein said additional memory comprises protective means for protection from the electromagnetic radiation.

43. An integrated circuit according to Claim 40, wherein said additional memory comprises input means for cooperating with said input/output means for storing the plurality of microinstructions therein.

44. An integrated circuit according to Claim 40, wherein said input/output means comprises a first path for serially transferring the command signal, and a second path for serially transferring the data and the address signals.

45. An integrated circuit according to Claim 44, wherein said memory control means comprises first serial/parallel conversion means connected to the first path and to said decoder means for a serial/parallel conversion of the command signal.

46. An integrated circuit according to Claim 44, wherein said memory control means comprises second serial/parallel conversion means connected to the second path and to said electrically programmable non-volatile memory for a serial/parallel conversion of the data and address signals.

47. An integrated circuit according to Claim 45,

wherein said memory control means further comprises bypass means that is selectively activated and is connected to said first serial/parallel conversion means and said additional memory for bypassing said decoder means so that the plurality of microinstructions being supplied to the first path and leaving said first serial/parallel conversion means is supplied directly to said electrically programmable non-volatile memory.

48. An integrated circuit according to Claim 47, wherein said bypass means comprises switching means including an output connected to said electrically programmable non-volatile memory, and said switching means includes a first operating state corresponding to connection of the output to said additional memory, and including a second operating state corresponding to connection of the output to said first serial/parallel conversion means.

49. An integrated circuit according to Claim 48, wherein said bypass means further comprises command means for switching said switching means between the first and second operating states.

50. A memory card for storing data, and for operating in cooperation with at least one of an external acquisition system and an external processing system, the memory card comprising:

a casing; and

an integrated circuit carried by said casing for storing the data, said integrated circuit comprising a non-volatile electrically programmable memory that is erasable by

exposure to electromagnetic radiation for permitting a non-electrical erasure of the stored data;

said casing comprising transparent means adjacent said non-volatile electrically programmable memory that is transparent to the electromagnetic radiation.

51. A memory card according to Claim 50, wherein the electromagnetic radiation comprises ultraviolet radiation.

52. A memory card according to Claim 50, wherein said transparent means includes an aperture in said casing exposing a portion of said non-volatile electrically programmable memory to the electromagnetic radiation.

53. A memory card according to Claim 52, further comprising polyaniline carried by the aperture for protecting said non-volatile electrically programmable memory.

54. A memory card according to Claim 50, wherein said casing further comprises reversible closing means for closing the aperture for protecting said non-volatile electrically programmable memory from undesired electromagnetic radiation.

55. A memory card according to Claim 54, wherein said reversible closing means comprises an adhesive element that is removable with respect to the aperture.

56. A memory card according to Claim 50, wherein said electrically programmable non-volatile memory comprises a first terminal for receiving a programming signal for enabling

storage of the data, and a second terminal for receiving a reading signal for enabling output of the stored data; and wherein said integrated circuit comprises:

input/output terminals for receiving the data to be stored from at least one of the external acquisition system and the external processing system, for sending the stored data to the external processing system, and for receiving a command signal from at least one of the external acquisition system and the external processing system; and

a memory control circuit connected to the first and second terminals of said electrically programmable non-volatile memory, and to said input/output means for generating the programming and reading signals based upon the command signal.

57. A memory card according to Claim 56, wherein said memory control circuit comprises:

an additional memory for storing a plurality of microinstructions for controlling said electrically programmable non-volatile memory; and

a decoder connected to said additional memory for converting the command signal to a selection signal for selecting at least one microinstruction.

58. A memory card according to Claim 57, wherein said integrated circuit comprises a first path connected to said input/output terminals for serially transferring the command signal, and a second path connected to said input/output terminals for serially transferring the data and address signals.

59. A memory card according to Claim 58, wherein said memory control circuit comprises a first serial/parallel conversion circuit connected to the first path and to said decoder for a serial/parallel conversion of the command signal.

60. A memory card according to Claim 58, wherein said memory control circuit comprises a second serial/parallel conversion circuit connected to the second path and to said electrically programmable non-volatile memory for a serial/parallel conversion of the data and address signals.

61. A memory card according to Claim 59, wherein said memory control circuit further comprises a bypass circuit that is selectively activated and is connected to said first serial/parallel conversion circuit and to said additional memory for bypassing said decoder so that the plurality of microinstructions being supplied to the first path and leaving said first serial/parallel conversion circuit is supplied directly to said electrically programmable non-volatile memory.

62. A memory card according to Claim 61, wherein said bypass circuit comprises a multiplexer including an output connected to said electrically programmable non-volatile memory, and said multiplexer includes a first operating state corresponding to connection of the output to said additional memory, and includes a second operating state corresponding to connection of the output to said first serial/parallel conversion circuit.

63. A system for acquiring sounds/images, the system comprising:

transducer means for generating an analog signal based upon the acquired sounds/images;

analog/digital conversion means connected to said transducer means for converting the analog signal into a digital signal;

a memory card being removably associated with said analog/digital conversion means for storing the digital signal as data, said memory card comprising

a casing, and

an integrated circuit carried by said casing for storing the data, said integrated circuit comprising a non-volatile electrically programmable memory that is erasable by exposure to electromagnetic radiation for permitting a non-electrical erasure of the stored data,

said casing comprising transparent means adjacent said non-volatile electrically programmable memory that is transparent to the electromagnetic radiation.

64. A system according to Claim 63, wherein the electromagnetic radiation comprises ultraviolet radiation.

65. A system according to Claim 63, wherein said transparent means includes an aperture in said casing exposing a portion of said non-volatile electrically programmable memory to the electromagnetic radiation.

66. A system according to Claim 65, further

comprising polyaniline carried by the aperture for protecting said non-volatile electrically programmable memory.

67. A system according to Claim 63, wherein said casing further comprises reversible closing means for closing the aperture for protecting said non-volatile electrically programmable memory from undesired electromagnetic radiation.

68. A system according to Claim 67, wherein said reversible closing means comprises an adhesive element that is removable with respect to the aperture.

69. A system according to Claim 63, wherein said electrically programmable non-volatile memory comprises a first terminal for receiving a programming signal for enabling storage of the data, and a second terminal for receiving a reading signal for enabling output of the stored data; and wherein said integrated circuit comprises:

input/output terminals for receiving the data to be stored; and

a memory control circuit connected to the first and second terminals of said electrically programmable non-volatile memory, and to said input/output means for generating the programming and reading signals based upon the command signal.

70. A system according to Claim 69, wherein said memory control circuit comprises:

an additional memory for storing a plurality of microinstructions for controlling said electrically programmable non-volatile memory; and

a decoder connected to said additional memory for converting the command signal to a selection signal for selecting at least one microinstruction.

71. A system according to Claim 69, wherein said integrated circuit comprises a first path connected to said input/output terminals for serially transferring the command signal, and a second path connected to said input/output terminals for serially transferring the data and address signals.

72. A system according to Claim 71, wherein said memory control circuit comprises a first serial/parallel conversion circuit connected to the first path and to said decoder for a serial/parallel conversion of the command signal.

73. A system according to Claim 71, wherein said memory control circuit comprises a second serial/parallel conversion circuit connected to the second path and to said electrically programmable non-volatile memory for a serial/parallel conversion of the data and address signals.

74. A system according to Claim 72, wherein said memory control circuit further comprises a bypass circuit that is selectively activated and is connected to said first serial/parallel conversion circuit and to said additional memory for bypassing said decoder so that the plurality of microinstructions being supplied to the first path and leaving said first serial/parallel conversion circuit is supplied directly to said electrically programmable non-volatile

memory.

75. A system according to Claim 74, wherein said bypass circuit comprises a multiplexer including an output connected to said electrically programmable non-volatile memory, and said multiplexer includes a first operating state corresponding to connection of the output to said additional memory, and includes a second operating state corresponding to connection of the output to said first serial/parallel conversion circuit.

76. An adapter device for interfacing a memory card with a processing system, the adapter device comprising:

a casing for receiving the memory card, and comprising electrical terminals for connection therewith;

interfacing means carried by said casing and connected to said electrical terminals for interfacing with the processing system, and for transferring stored data in the memory card to the processing system; and

an electromagnetic radiation source carried by said casing and positioned adjacent the memory card for erasing the stored data when the memory card is received by said casing.

77. An adapter device according to Claim 76, wherein said electromagnetic radiation source comprises a lamp that emits ultraviolet radiation.

78. An adapter device according to Claim 76, further comprising reflective means for guiding the electromagnetic radiation towards the memory card.

79. An adapter device according to Claim 76, wherein said casing is sized so that it is received by a socket of the processing system.

80. An adapter device according to Claim 76, wherein said interfacing means is defined in accordance with a PCMCIA-JEIDA standard.

81. An adapter device according to Claim 76, further comprising signal indicating means for signaling an operating state.

82. An adapter device according to Claim 76, wherein said interfacing means comprises a plug for connecting to a Universal Serial Bus (USB) port of the processing system.

83. A process for storing data in a memory card that operates in cooperation with at least one of an external acquisition system and an external processing system, the memory card comprising a casing, and an integrated circuit carried by the casing for storing the data, the integrated circuit comprising a non-volatile electrically programmable memory that is erasable by exposure to electromagnetic radiation for permitting a non-electrical erasure of the stored data, the casing comprising transparent means adjacent the non-volatile electrically programmable memory that is transparent to the electromagnetic radiation, the process comprising:

converting sounds/images acquired by the external acquisition system into an analog signal;

converting the analog signal into a digital signal;

and

transferring the digital signal to the memory card for storing as digital data.

84. A process according to Claim 83, further comprising erasing the stored data by exposing a portion of the non-volatile electrically programmable memory to electromagnetic radiation through the transparent means.

85. A process according to Claim 83, wherein the electromagnetic radiation comprises ultraviolet radiation.

86. A process according to Claim 83, wherein the transparent means includes an aperture in the casing for exposing a portion of the non-volatile electrically programmable memory to the electromagnetic radiation.

87. A process according to Claim 86, further comprising polyaniline carried by the aperture for protecting the non-volatile electrically programmable memory.

88. A process according to Claim 83, further comprising closing the aperture for protecting the non-volatile electrically programmable memory from undesired electromagnetic radiation.

89. A process according to Claim 83, wherein the electrically programmable non-volatile memory comprises a first terminal for receiving a programming signal for enabling storage of the data, and a second terminal for receiving a reading signal for enabling output of the stored data; and

wherein the integrated circuit comprises:

input/output terminals for receiving the data to be stored from at least one of the external acquisition system and the external processing system, for sending the stored data to the external processing system, and for receiving a command signal from at least one of the external acquisition system and the external processing system; and

a memory control circuit connected to the first and second terminals of the electrically programmable non-volatile memory, and to the input/output means for generating the programming and reading signals based upon the command signal.

90. A process according to Claim 89, wherein the memory control circuit comprises:

an additional memory for storing a plurality of microinstructions for controlling the electrically programmable non-volatile memory; and

a decoder connected to the additional memory for converting the command signal to a selection signal for selecting at least one microinstruction.

91. A process according to Claim 90, wherein the integrated circuit comprises a first path connected to the input/output terminals for serially transferring the command signal, and a second path connected to the input/output terminals for serially transferring the data and address signals.

92. A process according to Claim 91, wherein the memory control circuit comprises a first serial/parallel conversion circuit connected to the first path and to the

decoder for a serial/parallel conversion of the command signal.

93. An integrated circuit according to Claim 91, wherein the memory control circuit comprises a second serial/parallel conversion circuit connected to the second path and to the electrically programmable non-volatile memory for a serial/parallel conversion of the data and address signals.

94. A process according to Claim 92, wherein the memory control circuit further comprises a bypass circuit that is selectively activated and is connected to the first serial/parallel conversion circuit and to the additional memory for bypassing the decoder so that the plurality of microinstructions being supplied to the first path and leaving the first serial/parallel conversion circuit is supplied directly to the electrically programmable non-volatile memory.

95. A process according to Claim 94, wherein the bypass circuit comprises a multiplexer including an output connected to the electrically programmable non-volatile memory, and the multiplexer includes a first operating state corresponding to connection of the output to the additional memory, and includes a second operating state corresponding to connection of the output to the first serial/parallel conversion circuit.

REMARKS

It is believed that all of the claims are patentable over the prior art. For better readability and the Examiner's

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convenience, the newly submitted claims differ from the translated counterpart claims which are being canceled. The newly submitted claims do not represent changes or amendments that narrow the claim scope for any reason related to the statutory requirements for patentability. Accordingly, after the Examiner completes a thorough examination and finds the claims patentable, a Notice of Allowance is respectfully requested in due course. Should the Examiner determine any minor informalities that need to be addressed, he is encouraged to contact the undersigned attorney at the telephone number below.

Respectfully submitted,

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EXPRESS MAIL NO: EL747059113US

DATE OF DEPOSIT: June 14, 2001

NAME: Kyle Hopkinson

SIGNATURE:

SUBMISSION OF PROPOSED MODIFICATIONS TO DRAWINGS

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Submitted herewith is a request for proposed drawing modifications as indicated in red ink to label the blocks in FIGS. 1, 4-6, 8a-8b and 10. FIG. 10 is being further modified as indicated in red ink to correct a reference numeral.

Respectfully submitted,

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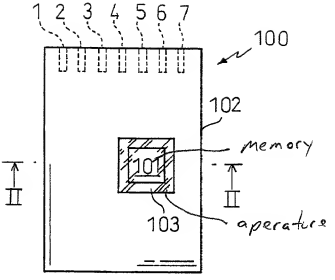

FIG.1

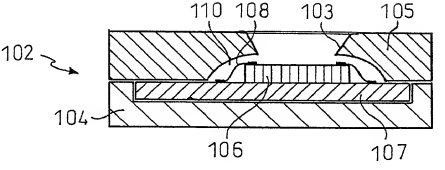

FIG.2

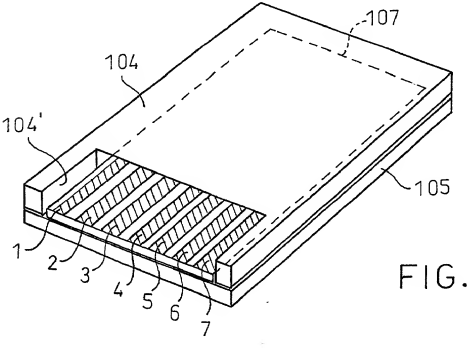

FIG.3

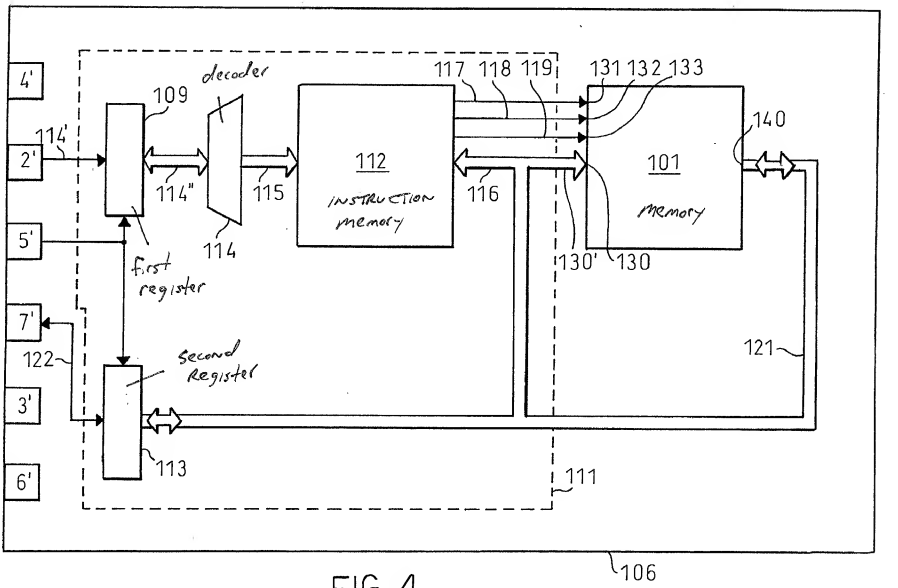

FIG. 4

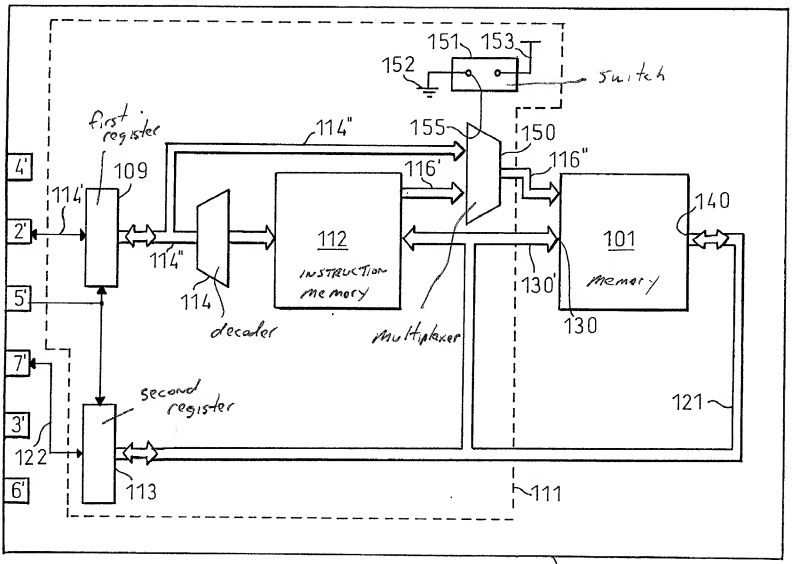

FIG. 5

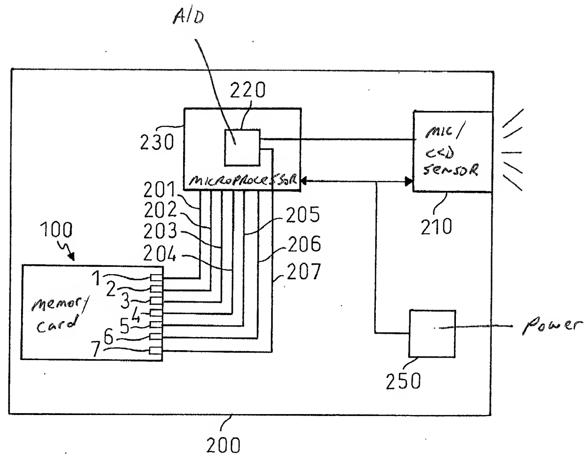

FIG.6

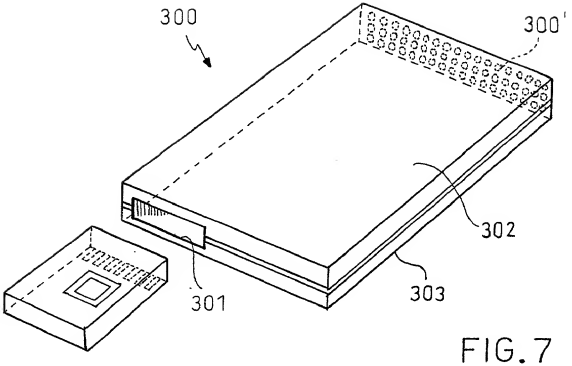

FIG. 7

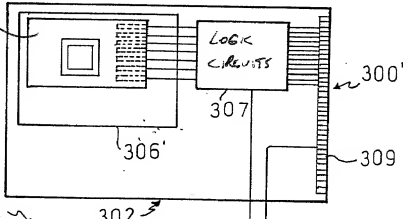

FIG. 8a

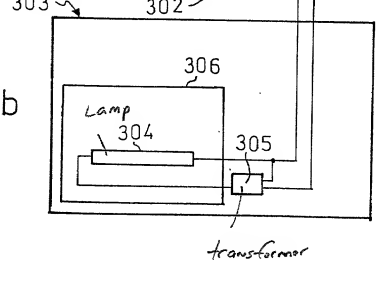

FIG. 8b

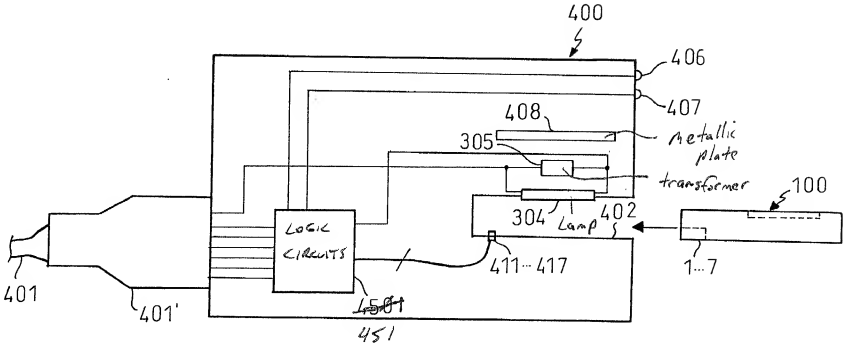

FIG.10